Advanced Verification Techniques: A SystemC Based Approach for Successful Tapeout

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"As chip size and complexity continues to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages. Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques, provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks."

- Stuart Swan

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